	ISSUE CLASSIFICATION	
Subclass		
Class		

PATENT NUMBER

U.S. UTILITY Patent Application

	O.I.P.E.	PATENT DATE
SCANNED	Q.A.	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER VERBRUGGE
09/558377	F	709 711	141	2756 2183	Radmanabhan

APPLICANTS

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TITLE

Modular interconnection architecture for an expandable
multiprocessor machine, using a multilevel bus hierarchy and the
same building block for all the levels

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL			CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					
INTERNATIONAL CLASSIFICATION								
				☐ Continued on Issue Slip Inside File Jacket				

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
	(Assistant Examiner)		(Date)		
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
	(Primary Examiner)		(Date)		
☐ The terminal ____months of this patent have been disclaimed.				ISSUE BATCH NUMBER	
	(Legal Instruments Examiner)		(Date)		

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